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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ERIC B. KUSHNICK

Appeal 2009-001310
Application 09/824,898[1]
Technology Center 2100

Decided: January 19, 2010

Before LEE E. BARRETT, JEAN R. HOMERE, and STEPHEN C. SIU, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] Filed on April 2, 2001. The real party in interest is Credence Systems Corp. (App. Br. 1.)

I. STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) (2002) from the Examiner's final rejection of claims 1 through 8, 11, 20 through 27, 30, 34, and 35. (App. Br. 1.)[2] Claims 9, 10, 12 through 14, 28, 29, 31 through 33, and 36 through 38 are objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. (Non-Final Rej. 7.)[3] Claims 15 and 16 have been cancelled. (App. Br. 1.) Claims 17 through 19 have been allowed. (*Id.*) We have jurisdiction under 35 U.S.C. § 6(b) (2008).

We reverse.

Brief Summary of The Invention

Appellant invented a method and apparatus that utilizes a high resolution programmable clock signal generator to provide a clock signal selected from a set of timing signals. (Spec. 1, Para. [0001].) Appellant's Figure 5 depicts a clock signal generator (50) containing a first coarse delay circuit (54) that "adjustably delays pulses of a ring oscillator ("ROSC") signal over a range spanning at least T_p seconds with a resolution of T_p/N in order to provide output CLOCK signal pulses." (Spec. 7, Para. [00029].) Additionally, the clock signal generator (50) contains a second coarse delay circuit (56) that "adjustably delays the CLOCK signal pulses over a range spanning T_p seconds with a resolution of T_p/M to provide pulses of the output CLOCK' signal." (*Id.*) In particular, "clock signal generator (50) can

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[2] All references to the Appeal Brief are to the Appeal Brief filed on August, 31, 2007, which replaced the prior Appeal Briefs filed on July 23, 2007, April 4, 2007, December 6, 2006, October 17, 2006, and October 2, 2006.
[3] Non-Final Rejection filed December 22, 2006.

be programmed to produce a variety of different CLOCK' signal periods by appropriately delaying selected ROSC signal pulses." (Spec. 9, Para. [00034].) Thus, according to the Appellant, the objective of the claimed invention is to provide a self-calibrating clock signal generator with a high period resolution. (Spec. 5, Para. [00015].)

Illustrative Claim

Independent claim 1 further illustrates the invention as follows:

> 1. An apparatus for generating pulses of a third pulse sequence in response to pulses of a periodic first pulse sequence having a period T_p, wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than period T_p, the apparatus comprising:
>
> first means for generating each pulse of a second pulse sequence in response to a separate pulse of the first pulse sequence with a first delay adjustable by first control data with a resolution of T_p/N over a first range substantially wider than T_p/M, wherein M and N are differing integers greater than one;
>
> second means for generating each pulse of the third pulse sequence in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data with a resolution of T_p/M over a second range substantially wider than T_p/N; and
>
> a programmable sequencer for changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary repetitively in a programmably adjustable manner.

Prior Art Relied Upon

The Examiner relies on the following prior art as evidence of unpatentability:

Hondeghem	4,255,790	Mar. 10, 1981
Heyne	6,194,928 B1	Feb. 27, 2001

J. CHRISTIANSEN ET AL., A TIMING, TRIGGER AND CONTROL DISTRIBUTION RECEIVER ASIC FOR LHC DETECTORS, TTCRX REFERENCE MANUAL, V. 2.2 (1997) (hereinafter "Christiansen").

Rejections on Appeal

The Examiner rejects the claims on appeal as follows:

Claims 1, 2, 4 through 8, 11, 20, 21, 23 through 27, 30, 34, and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Hondeghem and Christiansen.

Claims 3 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Hondeghem, Christiansen, and Heyne.

Appellant's Contentions

Appellant contends that Christiansen's disclosure of a deskew circuit that delays clock signals CLK01 and CLK02 to compensate for the inherent transmission line and processing delays in the path between the transmitter and receiver does not teach that transmission and processing delays in such a path vary in any repetitive manner. (App. Br. 17-22.) Further, Appellant alleges that Hondeghem's disclosure of a central processing unit ("CPU") (70), random access memory ("RAM") (84), and input/output ("I/O") logic (112), in conjunction with conveying data on lines (116) and (118), does not teach a sequencer that produces repetitively varying control data on lines (116) and (118) in response to an input pulse sequence. (*Id.* at 22-23; Reply Br. 1-3.) Additionally, Appellant contends: (1) there is insufficient rationale for the proffered combination; (2) Hondeghem and Christiansen are not within the scope of the prior art analogous to the claimed invention; and (3) the combination of Hondeghem and Christiansen is impermissible

because Hondeghem would render Christiansen inoperable for its intended purpose. (App. Br. 23; Reply Br. 3-6.)

Examiner's Findings and Conclusions

The Examiner finds that Hondeghem's disclosure of repetitively programming the system (i.e., CPU (70), RAM (84), and I/O logic (112)) and corresponding frequency selector (108) via lines (116) and (118) teaches a programmable sequencer that varies repetitively the control data in a programmable adjustable manner. (Ans. 8-9; 11.) Further, the Examiner finds that: (1) Hondeghem and Christiansen are within the scope of the prior art analogous to the claimed invention; and (2) there is sufficient rationale for the proffered combination. (*Id.* at 10.)

II. ISSUE

The pivotal issue before us is therefore whether Appellant has shown that the Examiner erred in concluding that that the combination of Hondeghem and Christiansen renders independent claim 1 unpatentable? In particular, the issue turns on whether the proffered combination teaches "a programmable sequencer for changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary repetitively in a programmable adjustable manner," as recited in independent claim 1.

III. FINDINGS OF FACT

The following Findings of Fact ("FF") are shown by a preponderance of the evidence.

Hondeghem

1. Hondeghem generally relates to a system that "generates output pulses in successive periods of time, each including sub-intervals during which the output pulses may vary in accordance with a pre-determined scheme." (Abst.)

2. Hondeghem's Figure 2 depicts a block diagram of a waveform generating system. (Col. 4, ll. 62-64.) Hondeghem discloses that "[t]he front panel board (52) includes a plurality of keyboard switches (62) responsive to key pad (12) … and connected to … I/O logic circuits (64) as indicated at (66)." (Col. 5, ll. 1-4.) "The I/O logic circuit (64) interfaces with the CPU (70) on the CPU board (54) as indicated at (72)." (*Id.* at ll. 6-8.) Additionally, "[a] crystal oscillator (74) interfaces with CPU (70) as indicated at (76)." (*Id.* at ll. 8-9.) "A plurality of data lines indicated at (82) connects the CPU (70) to a sequence random access memory (84) on RAM board (56), in which waveform sequence information is stored and retrieved in response to commands from CPU (70)." (*Id.* at 11-15.)

3. Additionally, Hondeghem discloses that "CPU (70) interfaces with I/O logic circuit (112) as indicated at (114)." (*Id.* at ll. 31-32.) "I/O logic circuit (112) supplies signals from the CPU (70) to the circuit elements on the timer board (58)." (*Id.* at 32-33.) "The I/O logic circuits (112) are connected to the period frequency selector (108) and the sub-interval frequency selector (110) by means of lines (116) and (118), respectively." (*Id.* at ll. 34-36.) Further, Hondeghem discloses that the system "can provide both highly complex and variable pulse sequences in accordance with a user program incorporating branching decisions." (Col. 6, ll. 54-57.)

IV. PRINCIPLES OF LAW

Obviousness

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("'On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.'" (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998))).

V. ANALYSIS

Claim 1

Independent claim 1 recites, in relevant part, "a programmable sequencer for changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary repetitively in a programmable adjustable manner."

As detailed in the Findings of Fact section above, Hondeghem discloses a system that generates output pulses in successive periods of time and which vary according to a pre-determined scheme. (FF 1.) In particular, Hondeghem's Figure 2 depicts a system that includes a keyboard connected to an I/O logic circuit that interacts with a CPU which interfaces with an oscillator and RAM. (FF 2.) Further, Hondeghem also discloses that a second I/O logic circuit interfaces with the CPU and is connected to a period frequency selector and sub-interval frequency selector. (FF 3.) In accordance with a respective user program, Hondeghem's period frequency

selector and sub-interval frequency selector output complex and variable pulse sequences received from the oscillator via the CPU and the corresponding I/O logic circuit. (FF 2-3.) We find that Hondeghem's disclosure teaches a system capable of being programmed to adjust respective pulse signals in order to output variable pulse signals and the data corresponding therewith.

However, we agree with Appellant that Hondeghem fails to teach or suggest a programmable sequencer, let alone a programmable sequencer that repetitively varies data in a programmable adjustable manner. (App. Br. 22-23; Reply Br. 1-2.) Although we find that Hondeghem's system may be programmed to adjust pulse signals in order to output variable pulse signals and the data corresponding therewith, Hondeghem's cited disclosure does not teach a specific programmable logic device or an electronic component capable of performing this function. Absent a showing that Hondeghem's disclosure contains a specific programmable logic device or an electronic component capable of being calibrated to repetitively vary pulse signals, we find that the Examiner has improperly relied upon Hondeghem's disclosure to teach the disputed limitation. Further, we find that Christiansen does not cure the noted deficiencies of Hondeghem.

Additionally, we note that the rationale provided by the Examiner does not explain why it would have been obvious to modify Hondeghem in view of Christiansen to arrive at the claimed invention. In particular, we fail to see how the Examiner's rationale of incorporating Christiansen's high-resolution pulse sequences into Hondeghem's system (Ans. 10) pertains to Appellant's claimed self-calibrating clock signal generator with a high period resolution.

Since Appellant has shown at least one error in the rejection of independent claim 1, we need not reach the merits of Appellant's other arguments. It follows that Appellant has shown that the Examiner erred in concluding that the combination of Hondeghem and Christiansen renders independent claim 1 unpatentable.

Claims 2 through 8, 11, 20 through 27, 30, 34, and 35

Because claims 2 through 8, 11, 20 through 27, 30, 34, and 35 also recite the limitation discussed above, we find that Appellant has also shown error in the Examiner's rejection of these claims for the reasons set forth in our discussion of independent claim 1.

VI. CONCLUSION OF LAW

Appellant has shown that the Examiner erred in rejecting claims 1, 2 through 8, 11, 20 through 27, 30, 34, and 35 as being unpatentable under 35 U.S.C. § 103(a).

VII. DECISION

We reverse the Examiner's decision to reject claims 1 through 8, 11, 20 through 27, 30, 34, and 35.

REVERSED

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